REMARKS

In the Office Action, Claims 1-36 are pending and presented for examination. Claims 1-4, 8-14, 18-21, 26 and 31-36 are rejected and Claims 5-7, 15-17, 22-25 and 27-30 are objected to. In this Response, Claims 1, 5, 10, 11, 12, 15, 21, 26, 31, and 34 are amended. Applicants respectfully request reconsideration of pending Claims 1-36 in view of the following remarks.

I. Specification Objections

The specification is objected to because of informalities. In response, Applicants have amended the specification as suggested by the Examiner. In view of such amendments, Applicants respectfully request that the Examiner withdraw the objection to the specification.

II. Claim Objections

Claims 5, 10, 15, 20, and 21 are objected to because of informalities. In response, Applicants have amended Claims 5, 10, 15, 20, and 21 as suggested by the Examiner. In view of Applicant's amendments to such claims, Applicant respectfully requests that the Examiner reconsider and withdraw the objection to Claims 5, 10, 15, 20, and 21.

III. Claim Rejections Under 35 U.S.C. §102(b)

Claims 1, 11, 21, 26, 31 and 34 are rejected under 35 U.S.C. §102(b) as being anticipated by Lakshmanamurthy et al. (*Network Processor Performance Analysis Methodology"*, Aug. 15, 2002, Intel Technology Journal) ("Lakshmanamurthy.") Applicants respectfully disagree with the Examiner's assertions and characterizations of the cited reference.

Claim 1 recites:

> 1. A method comprising:
> configuring one or more processors into a D-stage processor pipeline;
> transforming a sequential network application program into D-pipeline stages that collectively perform the sequential packet processing stage (PPS) of the sequential network application program; and
> executing the D-pipeline stages in parallel within the D-stage processor pipeline to provide parallel execution of the sequential network application program. (Emphasis added.)

Lakshmanamurthy is generally directed to a network processor performance analysis methodology that is developed to analyze the performance of various networking applications that are targeted for running on the IXP 2400 network processor. (See Abstract.) In contrast with Claim 1, Lakshmanamurthy does not disclose or suggest transforming a sequential network application program into D-pipeline stages that collectively perform the sequential packet processing stage (PPS) of a sequential network application program, as in Claim 1. Lakshmanamurthy does disclose the use of a data movement model to estimate the use of compute cycles and total I/O references required for the various operations performed by a network processor on each received packet, as well as an estimation of the total budget for the packet processing to determine how functional blocks are mapped onto available hardware resources and how software concepts are used to meet the performance goals, where the methodology is validated by implementing microcode and tuning the code on a simulator and hardware to demonstrate line-rate performance. (See page 20, left column, lines 10-47.)

Apposite to Claim 1, we submit that such disclosure of Lakshmanamurthy is directed to determining the performance analysis that would be available to a hypothetical target application if implemented to use the parallel architecture of an IXP 2400 network processor. Lakshmanamurthy does disclose implementing microcode and turning the code on simulated hardware to demonstrate line-rate performance based on a data movement model, an estimated number of compute cycles, and total I/O references required for operations performed on a packet basis, as well as a total available budget for packet processing to enable performance analysis of a hypothetical target application that can be written to run on an IXP 2400 network processor (see Supra), however, that is something completely different from transforming a sequential network application program into D-pipeline stages that collectively perform the sequential packet processing stage (PPS) of the sequential network application, as in Claim 1.

Furthermore, Lakshmanamurthy fails to disclose or suggest executing the D-pipeline stages in parallel within the D-stage processor pipeline to provide parallel execution of the sequential network application program, as in Claim 1. According to the Examiner, this feature of Claim 1 is disclosed by the conclusion section at page 25 of Lakshmanamurthy. (See page 4-5 of the Office Action mailed 7/6/07.) However, the Examiner's characterizations of Lakshmanamurthy, as well as the conclusion section is directed to providing performance

analysis of a hypothetical network application that is targeted for running on an IXP 2400 network processor.

In contrast to Claim 1, we submit that Lakshmanamurthy presumes that a target application has been written for execution on the IXP 2400 network processor and based on such presumption, determines the efficiency with which such network processor may run the application based on the methodology described above. Hence, neither the sections referred to by the Examiner, nor any other disclosure of Lakshmanamurthy discloses or suggests transforming a sequential network application program into D-pipeline stages that collectively perform the sequential packet processing stage (PPS) of a sequential network application program, much less that the D-pipeline stages are executed in parallel within the D-stage processor pipeline to provide parallel execution of the sequential network application program, as in Claim 1.

For each of the above reasons, therefore, Claim 1, and all claims which depend on Claim 1, are patentable over the cited art.

Each of Applicant's other independent claims include features similar to those highlighted above in Claim 15. Therefore, all of Applicant's other independent claims, and all claims which depend on them, are also patentable over the cited art for similar reasons.

IV. Claim Rejections Under 35 U.S.C. § 103(a)

Claims 2, 12, 32, and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lakshmanamurthy in view of Rakhmatove et al., ("*Hardware-Software Bipartitioning for Dynamically Reconfigurable Systems*", *May 2002, ACM*) ("Rakhmatov.")

DEPENDENT CLAIMS

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

V. Allowable Subject Matter

Claims 5-7, 15-17, 22-25, and 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejections under 35 U.S.C. 102(b) and/or 35 U.S.C. 103(a) set forth to include all the limitations of the base claim and any intervening claims.

Applicants respectfully thank the Examiner for recognizing the allowability of Claims 5-7, 15-17, 22-25, and 27-30. However, for at least the reasons provided above, Applicants respectfully submit that such claims, based on their dependency from independent Claims 1 and 21, are also patentable over Lakshmanamurthy, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the objection to Claims 5-7, 15-17, 22-25, and 27-30, and allow such claims, based on their dependencies from Claims 1 and 21.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 10/5/07

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Elaine Kwak — 10/5/07 Date